3.12 Pixel Readout Electronics

The pixel detector is composed of about 1.5×10^8 pixels contained in about 3×10^4 front-end chips. The electronics is composed of two parts: — the on-detector and off-detector electronics. Figure 3.1 shows an example of the relationships among the major blocks of electronics. The function of the on-detector electronics is to detect hits, save them pending a Level 1 trigger and read out the hits defined by the trigger. The function of the off-detector electronics is to provide services (power and high voltage), clocks and control (commands such as trigger and control register values) for the on-detector electronics and the buffering of event data for transmission to the DAQ and Level 2 trigger processors. The numbers in this section, and in figure 3.1, are presented in the context of the LBL design and the data flow rates given in section 3.9, without the B-physics layer.

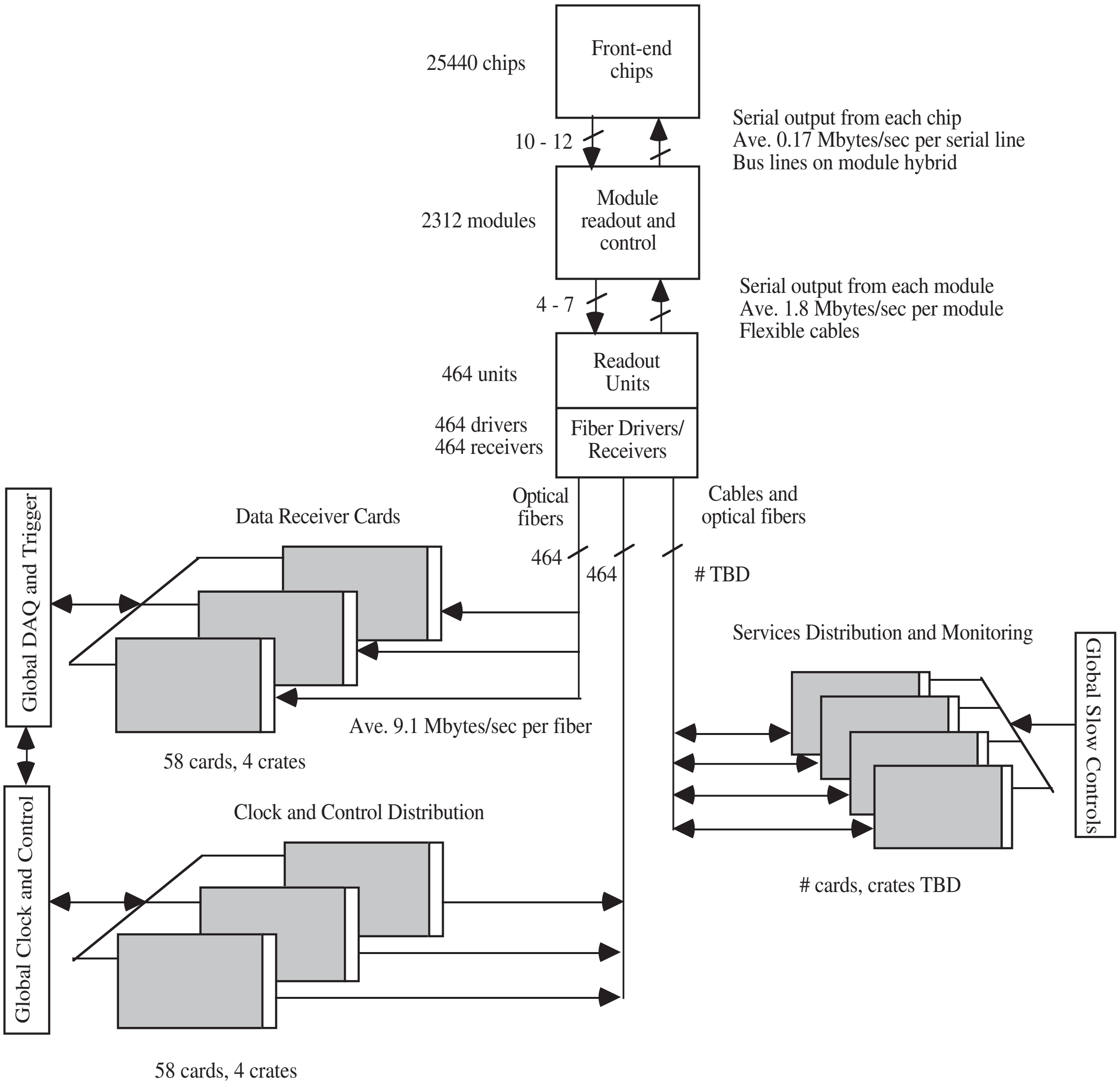

Figure 3.1: An example of the pixel data flow architecture

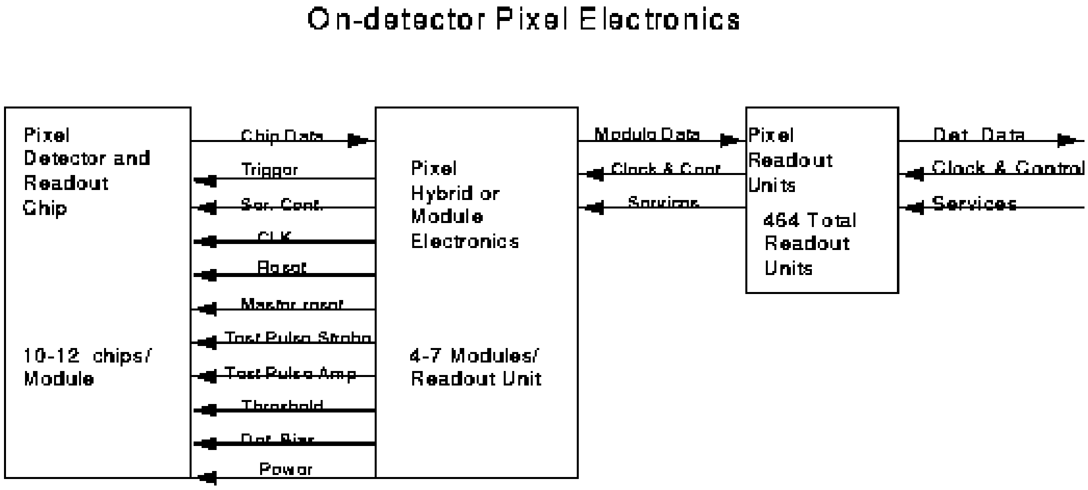

Figure 3.2: On-Detector Pixel Electronics.

3.12.1 Pixel Electronics On-Detector Basic Functionality

The on-detector electronics is comprised of the front-end chips, a smaller number of readout and control (ROC) chips and multiplexing electronics for input/output to/from optical fibers. The number of the multiplexing (readout units) is not yet well defined but we assume here that 4–6 ROCs will be included in each readout unit as defined in 3.9 — one-half of barrel stave and four disk wedges. After a Level 1 trigger accept, the data will be digitized and readout to the off-detector electronics. Other function that must be supported are test pulse injection and masking of defective channels or chips.

3.12.1.1 Interfaces to the On-Detector Electronics The interface is composed of the following items (see figure 3.2):

a. Data to the off-detector electronics. This data link is optical. The exact speed and number of links is under discussion, but we assume here the minimum number of links, which is about 500. If greater bandwith is required, additional fibers would be needed. These could be implemented as additional fibers per readout unit or by increasing the number of readout units e.g., one fiber per module. The difference between the two is a matter of the amount of multiplexing and resulting fiber speed. Functionality is the same for the options. Data rates for the minimum fiber option are given in section 3.9. Detector data are delivered by the fibers to receiver cards.

b. Clock, commands and control. This link is composed of optical fibers that contain the following information:

   1. Clock at the beam crossing frequency,
   2. Level 1 trigger,

3. Control information composed of reset, master reset, data to set control functions, etc. Definition and protocol of these signals is yet to be completed but the general classes of information given above must be supported.

c. Services

The services are composed of detector high voltage, DC power, analog level for control (test pulse amplitude and thresholds) and temperature monitors. It should be noted the analog levels could be generated in the on-detector electronics. Service cables will be designed to provide a minimum number of radiation lengths.

3.12.1.2 Pixel Readout Chip and Detector The electronics for the pixel front-end chip has been described previoulsy. Here we will assume that after a Level 1 trigger accept, a pixel column or the readout control will have stored the desired hits and their correlation to the 8 bit beam crossing counter. Functionality of the readout control and optional ADC circuitry is to gather the data from a given crossing and place it in a 32 bit $\times$ 64 deep FIFO. Data stored are a 6–8 bit amplitude, 8 bit crossing counter, 8 bit row location, 5 bit column number and 1 bit to indicate no data. The length and location of the buffer memories requires more optimization.

Data from the 32 $\times$ 64 FIFO are pushed to the next level of multiplexing in a serial format. Serial format has been picked to reduce the number of lines on the module hybrid. The derandomizing buffers in the front-end chips allows the serial lines from each front-end chip to be operated at a frequency as low as 10 MHz if needed and consistent with the average event rate. However, large events will require a readout time that exceeds $2^8 \times 25$ nsec $= 6.4\mu$sec, in which case the 8 bit crossing counter could repeat, potentially causing confusion in building events. The solution to this problem requires further study, but one cure would be to add more bits to identify the trigger time.

Control of registers (mask, test, etc.) is accomplished by a serial slow control link that provides for the setting of pixel masks, test pulse enables and counter offsets. Serial format has been chosen to reduce the number of lines on the hybrid.

3.12.1.3 Pixel Module Electronics There are approximately 2500 pixel modules. The pixel module electronics has two main functions. One is to receive the front-end readout data and build a mini-event. The other is to decode the clock and control data to support the pixel front-end chips. These functions are shown in figure 3.3. Services consisting of power, detector high voltage and analog voltages for test pulse amplitude and thresholds are fanned out to the front-end chips supported on a module. Clock and control is composed of several signals. There could be the following lines/signals: clock at the beam crossing frequency and 3 lines/bits of command (decoded as trigger, control with serial data following on these lines, strobe test pulse, reset, master reset, etc.). The exact details will be defined at a later time.

It is necessary for the pixel module electronics to know what the trigger identifiers are and what order they will arrive from the read out chips. This is accomplished by duplication of the 8 bit crossing counter with an offset that is used to validate a trigger on the readout chip in the 8 deep trigger FIFO that keeps track of triggers. Each data source is stored in a

32×64 word FIFO. Events are built and transmitted by circuitry that reads the next trigger number from the trigger FIFO. Then the data storage FIFOs are scanned for hits belonging to that trigger number. The hit data is transmitted from the module in serial format to the next layer of multiplexing. Four bits of address must be added by the module electronics to identify the chips on a module (total of 32 bits per word). If there is no data for one of the active inputs (time out) an error code is attached to the output data. The transmission rates and FIFO lengths need additional evaluation.

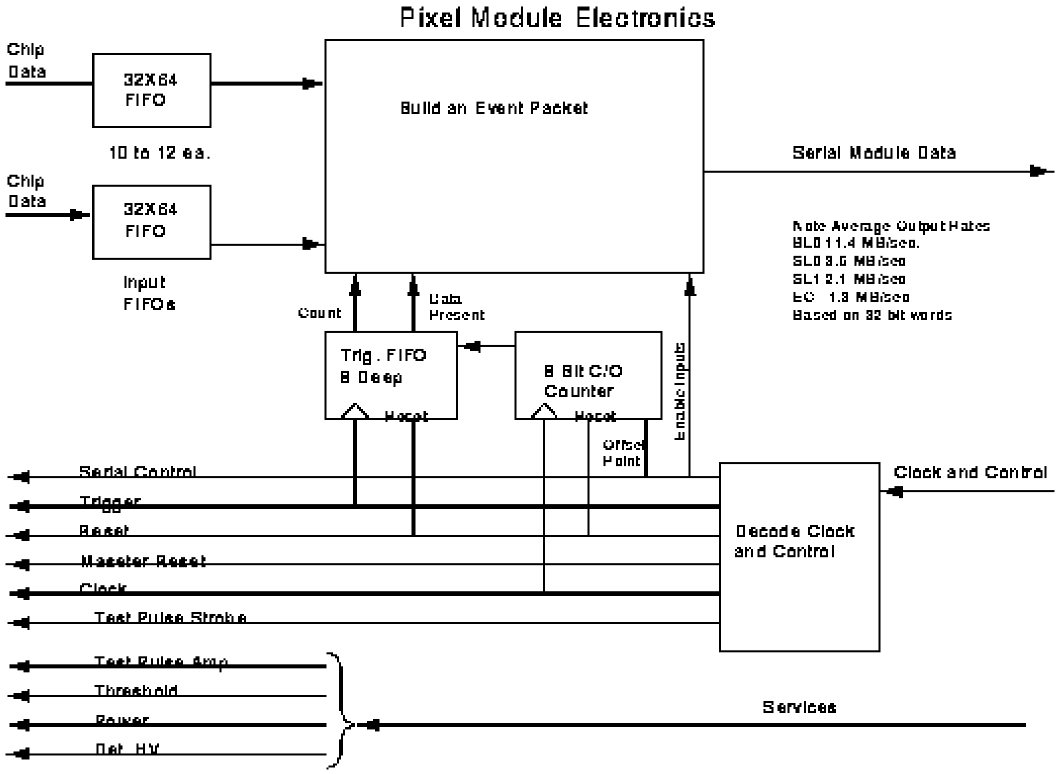

Figure 3.3: Pixel Module Electronics.

3.12.1.4 Pixel Readout Units The functionality of the circuitry is similar to the pixel module electronics described above. There are three differences. The input FIFO is 32 bits by 256 words deep to allow for the larger event size. Optical drivers have been added to the serial output. The speed of optical transmission and the degree of multiplexing are obviously related in this model. They effect the FIFO depth needed to derandomize the data.

3.12.2 Off-detector Electronics Basic Functionality

The pixel off-detector electronics provides three basic functions. One is to receive the on-detector data, buffer it and present it to the DAQ and Level 2 trigger. The second is to provide control signals such as trigger and register control. And the third is to provide power, biases and slow control monitoring.

3.12.2.1 Interfaces to the Off-Detector Electronics The interfaces to the on detector electronics are detailed in section 3.12.1.1. Interfaces to the rest of ATLAS are listed below:

a. Data to DAQ or Level 2 trigger

   These data links are expected to be optical and operate at about 1 giga-bit per second. There are about 200 of these links to carry the required bandwidth. The number depends on the level of multiplexing and the inclusion, or not, of the B physics layer at full luminosity. Each link will provide data from one event at a time. The format is yet to be defined, but it is essential that a unique identifier be attached to an event. If there is no data, a dummy event is sent.

b. ATLAS network

   This is a general purpose network that supports the activities in a crate. It has several function that include those listed below:

   1. down loading of programs,
   2. down loading of control information,
   3. monitoring of event data,
   4. slow controls functions such as setting of test pulse amplitudes,
   5. slow control function such as reading temperature,
   6. voltage and currents,
   7. and special instruction to the electronics.

c. ATLAS clock and control

   This is a high speed optical link the supports such global actions as are listed below:

   1. Level 1 trigger,
   2. master reset,
   3. reset,
   4. test pulse strobe,
   5. etc.

3.12.2.2 Pixel Receiver and Control Electronics The main function of the receiver card is to collect data from all of the inputs and present data to the DAQ and Level 2 trigger from each card. There could be 32 to 200 of these cards (58 in a model with 8 fibers per card, as in figure 3.1), since the number depends on the level of multiplexing and the number of fibers. At the highest level of multiplexing, the worst case would be one optical fiber to the DAQ for each input operating near the 1 giga-bit speed. This area needs analysis to find the best optimization of the required fiber speeds. These cards are crate based as shown in figure 3.1. The crate processor performs the function of general control, slow control, error monitoring and data sampling. Pixel clock and trigger distribution accepts the high speed ATLAS clock and control and interfaces the information to the receiver cards over the local clock and control bus.

The pixel receiver card is informed of an event over the local clock and trigger distribution bus. The control circuitry that is connected to the local clock and control bus informs the receiver circuitry. The data are gathered and transmitted as is the location to use in the linked list (see figure 3.4). There are 8 to 24 (space limit) data receiver circuits on a board. Each data receiver places the information from its input fiber in a dual ported memory. If no data are present, a dummy data word is saved in the dual ported memory. The functionalities of this operation are listed below:

- detect header(identify event),
- receive and format data,
- place data in dual ported memory and at the end of the data place pointers and header in the linked list.

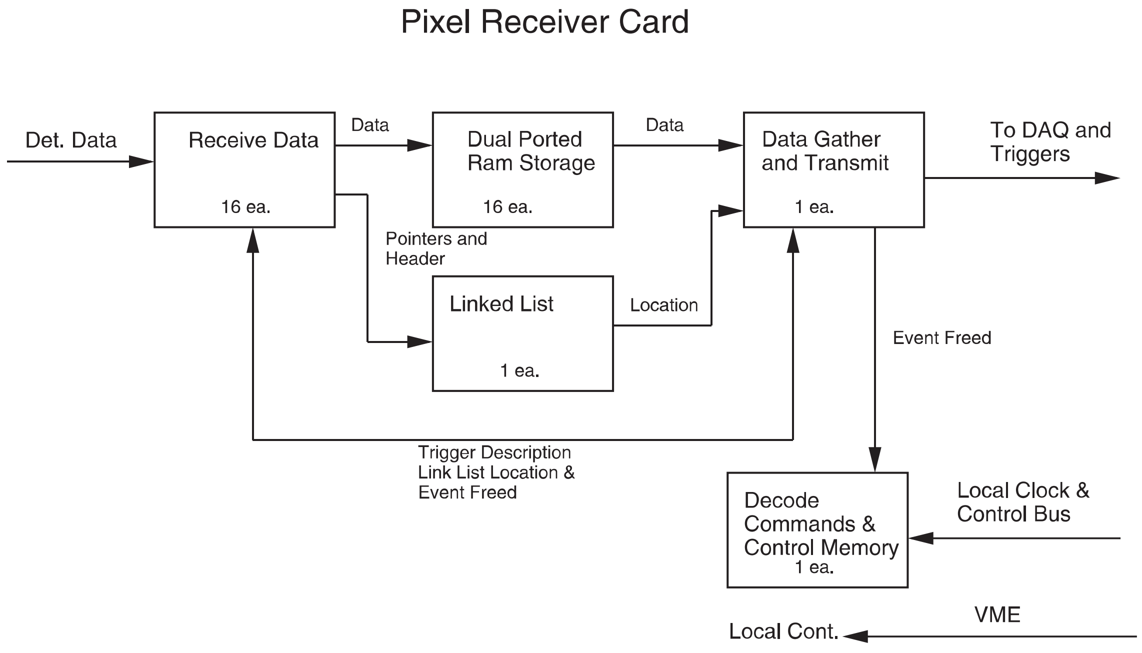

Figure 3.4: Pixel Receiver Card.

When all receivers have read and stored their data and pointer, the data- gather- and transmitter-circuit will read the linked list and extract the data from the dual ported memories. Four to five address bits are added to the data at this point. Data are pushed to the DAQ and Level 2 trigger over optical fibers. When all data have been transmitted to the DAQ, the control circuitry is informed. It informs the receivers to free the dual ported memory for that event.

The function of the pixel clock and trigger distribution card is to receive the high speed ATLAS clock and control optical information and distribute it over a local bus to the cards in the crate and the on-detector electronics. The high speed data are separated into three types of data. One is the clocks data type. Another is the serial control data type that is used for global commands. The last is crossing specific data type. Crossing specific data are then decoded into commands such as master reset, reset, Level 1 accept, strobe test pulser, etc. Clocks are phase adjusted to the local time frame. This information is distributed over the local crate bus to the card in the crate. The functionality above is generic and expected to evolve.

3.12.2.3 Pixel Service Electronics The pixel service electronics main function is to distribute voltages to the on-detector pixel electronics and to provide monitoring of these electronics. It is assumed that each card will support 16 read out units. The crate count is 2 to 13 crates depending on the level of multiplexing. Each crate has a processor and about 15 pixel service cards. The pixel DC and detector bias supplies feed through the pixel service cards. The processor performs the function of slow controls and monitoring of voltages, currents and temperatures.

The pixel service card can be thought of as a 1 to 16 distribution card. It takes the power and control data and distributes it. It has the circuitry to measure temperature and power voltages and generate analog voltages. The DACs may be located in the on-detector electronics.