Chapter 3

INNER DETECTOR

3.1 Overview and Specifications

The ATLAS inner detector (ID) is shown in Fig. 3.1. It occupies the cylindrical cavity defined by the boundaries of the electromagnetic-calorimeter cryostats, with a radius $R = 115$ cm and $|z| = 345$ cm. Polyethylene moderators are situated from $|z| = 340$ cm to $|z| = 345$ cm on the front face of the end-cap calorimeters to lower the energy of neutrons entering the cavity, thus reducing their damage to the detector. The cavity is enclosed in a solenoid with an axial central field of 2 T.

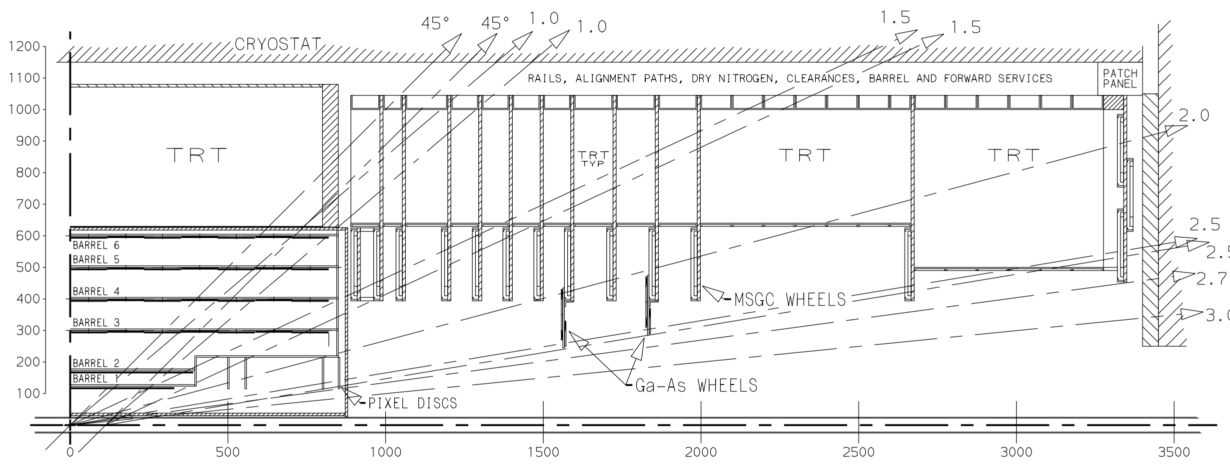

Figure 3.1: Layout of the ATLAS inner detector

The Inner Detector components are subject to large fluences of charged hadrons (mostly pions) and low energy neutrons and photons created in the calorimetry surrounding the ID. Radiation damage and other effects caused by the high flux of particles are important determining factors in the design of the ID. Inner detector components are expected to remain operational after three years of operation at a luminosity of $10^{33}\mathrm{cm}^{-2}\mathrm{sec}^{-1}$, followed by seven years of operation at $10^{34}\mathrm{cm}^{-2}\mathrm{sec}^{-1}$. The initial detector configuration will also contain a vertex-determining layer at a radius between 4 and 6 cm which will be removed after the first few years of operation.

The performance specifications of the inner detector for high-luminosity running are:

- Tracking coverage over the pseudorapidity range $|\eta| < 2.5$.
- Momentum resolution of $\Delta p_{\mathrm{T}}/p_{\mathrm{T}} < 30\%$ at $p_{\mathrm{T}} =$ 500 GeV for $|\eta| < 2$, and no worse than 50% for $|\eta| = 2.5$.
- Polar-angle resolution of < 2 mrad.
- Tracking efficiency of $> 95\%$ over the full coverage for isolated tracks with $p_{\mathrm{T}} > 5$ GeV, with fake-track rates less than 1% of signal rates.
- Tracking efficiency of $> 90\%$ for all tracks with $p_{\mathrm{T}} > 1$ GeV in a cone $\Delta R < 0.25$ around high-p_{T} isolated track candidates, with less than 10% of such tracks being fakes. Here, ΔR is defined as the separation of the particles in pseudorapidity–azimuth space.
- Electron-finding efficiency (integrated over all p_{T}, and including the trigger efficiency) of $> 90\%$ for a second electron with $p_{\mathrm{T}} > 0.5$ GeV near a high-p_{T} electron candidate, in order to suppress photon-conversion and Dalitz-decay backgrounds.
- High-p_{T} electron-identification efficiency above 90% both in the trigger and in the full reconstruction, including the effects of bremsstrahlung in the tracker material.
- Combined efficiency of the calorimeter and inner detector in excess of 85% for finding photons in the $p_{\mathrm{T}} \sim 60$ GeV range, with an electron rejection factor > 500 and with an isolated π^0 rejection factor > 3.
- Tagging of b jets with an efficiency $> 30\%$ at the highest luminosity, with a rejection > 10 against non-b hadronic jets.
- Measurement of the z coordinate of primary vertices with at least four charged tracks to better than 1 mm.
- Provision of a LVL2 track trigger to select isolated tracks with $p_{\mathrm{T}} > 20$ GeV with an efficiency $> 90\%$ and a fake track rate of $< 10\%$, in a cone of $\Delta R < 0.25$ around high-E_{T} e.m. calorimeter clusters.

During initial lower-luminosity running additional goals are:

- Tagging of b jets with an efficiency above 30%, with a rejection > 50 against non-b hadronic jets.
- Ability to reconstruct secondary vertices from b and τ decays
- Reconstruction of charged tracks from primary vertices and from secondary decay vertices of short-lived particles, with $> 95\%$ efficiency for $p_{\mathrm{T}} > 0.5$ GeV over the full coverage.

- Reconstruction efficiency > 90% for K^0_S decays with $p_T \sim 5$ GeV within a radius of 50 cm of the interaction point, integrated over radius.
- Reconstruction and identification of electrons with $p_T > 1$ GeV with an efficiency > 70%.

3.1.1 Layout

The layout of the inner detector aims to meet the above goals by applying a consistent design concept over the whole acceptance. This makes use of a combination of a few high-precision, high-granularity layers in the inner part of the tracker, and straw tubes in the outer part which supply a large number of measurements on the track trajectories. This concept offers the benefits to pattern recognition of a device which makes a large number of 'continuous' track measurements over a long track length, as well as those of a smaller number of higher-precision points.

The large track density requires the use of tracking layers with high granularity, and the momentum-resolution and spatial-resolution targets demand a high precision per point in both coordinates. Semiconductor devices on silicon or GaAs substrates, and microstrip gas counters (MSGC) offer such resolutions. A combination of pixel detectors and small-angle stereo-strip tracking provides the required granularity.

Table 3.1: Parameters of the inner detector. The values for the two low-luminosity vertexing layer options are given in parentheses.

System	Position	Area (m^2)	Resolution σ (μm)	Channels (10^6)	η coverage
Pixels	(1 low-lum. barrel layer) 2 barrel layers 4 forward disks on each side	(0.2) 1.4 0.8	($R\phi = 14, z = 87$) $R\phi = 14, z = 87$ $R = 87$	(12) 140	(± 2.5) ± 2.5
Silicon strips	(1 low-lum. barrel layer) 4 barrel layers	(0.2) 41	($R\phi = 10, z = 20$) $R\phi = 15, z = 770$	(0.03) 2.9	(± 2.1) ± 1.4
GaAs	2 forward disks on each side	3.3	$R\phi = 10, R = 1200$	0.8	2.0–2.5
MSGC	12 forward disks and 1 wheel on each side	51	$R\phi = 35, R = 1800$	1.5	1.4–2.5
TRT	Axial barrel straws Radial forward straws 36 straws per track		170 (per straw)	0.1 0.32	± 2.5

The parameters of the tracker are given in Table 3.1. Three detector types are deployed, in each case covering both the barrel and forward regions:

- **Pixel detectors** are used nearest to the beam pipe. The ATLAS pixel system includes two barrel layers and eight disk layers to provide at least two points for tracks with $|\eta| \lesssim 2.5$. These provide two-dimensional spatial information for pattern recognition and are expected to have an order-of-magnitude greater resistance to radiation damage than silicon-strip detectors. The radiation levels at the LHC preclude the long-term operation of silicon-strip detectors within a radius of about 30 cm and the charged-particle track density within this region is very high.

- **Strip detectors** are used for the larger-area precision trackers. High precision is obtained in the ϕ direction in both the barrel and in the forward regions. A lower precision is acceptable in the non-bending plane, and this is obtained by the use of small-angle stereo, which also gives a low fraction of ambiguous hits. Silicon detectors are foreseen in the barrel region, with GaAs substrates used in the region of highest fluence in the forward system, exploiting their higher radiation tolerance. Microstrip gas counters (MSGC) have been developed for the large-area forward strip detectors. A silicon option is also available for this region. Milestones have been defined for both forward-region options to demonstrate their performance and long-term viability. MSGCs will be used provided that they offer a clear performance/cost advantage, and a decision is anticipated by the end of 1995.

  The pixel, silicon and GaAs detectors together comprise the **Semi-Conductor Tracker (SCT)**. Each semiconductor-strip layer consists of two single-sided detectors glued back-to-back to measure alternating combinations of ϕ and u, or ϕ and v for the barrel, or combinations of u and v for the GaAs forward disks. Each MSGC disk, or 'layer', measures three coordinates (ϕ, u and v). A precision point may therefore consist of a single pixel hit, a pair of coordinates from the semiconductor strips, or a triplet from the MSGCs. Typically six precision points are provided over the full acceptance.

- **Straw tubes** are used at larger radii where the track density is relatively low, and the > 36 track points produced by about 64 closely-spaced layers can be used to best advantage for pattern recognition. Radiators are provided to generate transition radiation which gives additional electron-identification ability, independent of the energy–momentum matching between the calorimeter and tracker. This information is particularly useful at lower transverse momenta (< 5 GeV). The straw-tube system will generally be called the **Transition Radiation Tracker (TRT)** in this proposal.

- A **vertexing layer** is included in the SCT design. This removable layer around the beam pipe enhances significantly the vertex-finding capability for B physics and other physics during the first few years of LHC operation. This layer is foreseen as either an additional pixel layer at a radius of ~ 4 cm or a double-sided silicon-strip layer at ~ 6 cm.

3.2 SCT

The main requirements for the SCT are to provide powerful track-finding and pattern-recognition performance, a sagitta resolution of $\lesssim$ 25 μm, a polar-angle resolution of < 2 mrad, and b tagging using impact parameter measurements.

The design of the SCT is a compromise between two considerations:

- Minimizing the amount of material, cost and hence the number of layers and readout channels.

- Maintaining an adequate number of layers and readout granularity to facilitate track finding at high luminosity and within jets at lower luminosity.

Systematic studies have been made to guide the choices of the various design parameters by considering the way in which they affect pattern recognition, and they are briefly summarized below.

Detector efficiency has little effect on isolated leptons at low luminosity, but the track-finding efficiency falls by about 0.004 for each per-cent change in detector efficiency at $\mathcal{L} = 10^{34}$ cm^{-2} s^{-1} or in jets.

Noise above about 0.5% on the strip detectors degrades the pattern recognition, with the fake rate increasing rapidly and the efficiency falling.

The stereo angle between u/v and ϕ strips determines the number of ghost space-points which are reconstructed; the fake-track rate is minimized by reducing this angle. An angle of 40 mrad provides a good compromise between low fake rate and the requirements on z resolution needed to obtain good mass resolution.

The readout pitch affects the efficiency for reconstructing tracks in jets. Typically, hits separated by less than about three times the pitch, may not be resolved, and this provides an upper limit for the pitch. The track-reconstruction efficiency within jets is shown in Fig. 3.2.

The resolution quoted in Table 3.1 can be simply derived from the intrinsic detector precisions and the stereo angles. For the barrel silicon strips, 22 μm strip resolution with 40 mrad stereo angle results in a precision in $R\phi$ of 15 μm and 770 μm in z per measurement plane. However, these are not the 'effective' precisions to be used when fitting a helix, where the correlation between u and v planes effectively reduces the error in z to 540 μm. No systematic errors have been included — these could realistically be of the order of 10 μm after alignment.

3.2.1 Summary of Proposed US Responsibilities for ATLAS Pixel and Silicon Systems

Charged particle tracking in the ATLAS detector depends heavily on measurements using pixel and silicon strip detector devices. The U.S. ATLAS groups have been developing such detectors for over five years for use at high rate hadron colliders and they have much to contribute to ATLAS. Although much progress has been made on the technology needed to use pixel and silicon strip detectors on a large scale, all major aspects of the project — development of the detectors, electronics, data readout, modules which integrate the detector

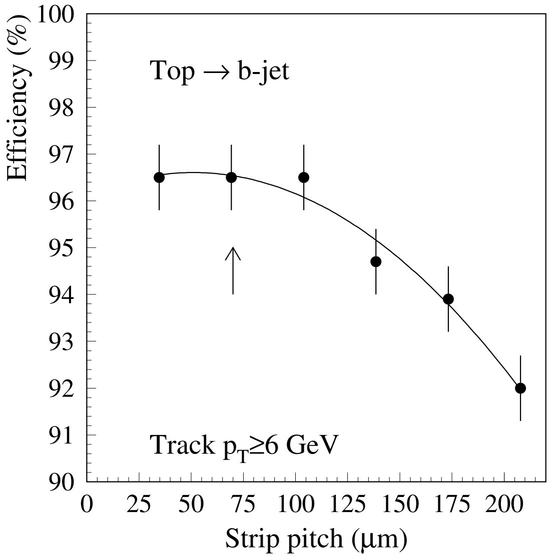

Figure 3.2: Track reconstruction efficiency in jets as a function of silicon-strip pitch

and electronics, cooling, and precision mechanical structures — need further R&D, particularly to provide a tracker designed to run for many years at a luminosity of $10^{34}\mathrm{cm}^{-2}\mathrm{sec}^{-1}$. Survival at these very high luminosities necessitates the use of pixels in the initial tracker configuration and requires strips to both be moved to larger radii and survive larger fluences than foreseen in the silicon trackers designed for the SSC.

The US institutions involved in the pixel and silicon strip systems, including the directly related aspects of the data acquisition/trigger, are LBL, UC Irvine, UC Santa Cruz, University of New Mexico and the University of Wisconsin. These groups (except for University of New Mexico which recently joined ATLAS) have been participating in the main ATLAS meetings since the beginning of calendar 1994 aimed at defining the electronics, detectors, module structure, readout scheme and overall geometry. Contributions have been made in all of the above areas. The plans below reflect initial discussions of responsibilities among the relevant ATLAS groups.

Pixel System

The University of California at Irvine, Lawrence Berkeley Laboratory, the University of New Mexico and the University of Wisconsin will seek to provide about 1/3 of the pixel detector system and a large fraction, possibly all, of the off-detector readout and control electronics. LBL is taking an important role in (a) the design, fabrication and testing of the front-end electronics readout; (b) design and fabrication of silicon detector elements; (c) design, fabrication and testing of multi-chip/detector modules; and (d) the mechanical/cooling system. LBL may also assemble modules into larger structures (barrels or disks) if it is necessary to do so. The University of New Mexico, which has very recently joined the ATLAS collaboration, would expect to take a substantial role in one or more of the above areas.

The University of Wisconsin, UC Irvine and LBL would collaborate on the design of readout and control electronics for the pixel system and will seek to provide all pixel readout and control boards. These institutes are now collaborating on preparing readout boards and modules for the LBL-4 pixel array in preparation for a beam test later this year.

Silicon Strip System

LBL, UC Irvine, UC Santa Cruz and Wisconsin will collaborate on the design, fabrication and testing of silicon modules and will seek to provide a substantial fraction of the off-detector readout and control electronics. The goal is to produce about 1/4 of the barrel silicon detector modules. If silicon strips are used in the forward region of the inner detector (disks), these modules might also be partially provided by LBL and UCSC. LBL and UCSC would expect to take an important role in (a) the design, fabrication and testing of some or all aspects of the front-end electronics; (b) the design, fabrication, and testing of modules; and (c) the conceptual design of the mechanical/cooling system. LBL and UCSC are willing to provide a substantial fraction, up to all, of the front-end electronics but are not seeking to procure or provide a significant fraction of the silicon detectors. This would be a cost effective arrangement, given the substantial work already done by LBL/UCSC on electronics and the presence of radiation hard chip processing in the US. Similarly, LBL/UCSC would be willing to provide a substantial fraction of other components that are necessary to construct modules.

LBL, UCSC, Irvine and Wisconsin will collaborate on the design of the off-detector electronics for the silicon strip system. Wisconsin and Irvine would share the fabrication of the silicon strip readout and control boards, which are expected to be very similar to those used for the pixel system.

Final Assembly

The pixel and silicon strip modules, produced at LBL and UCSC, as well as a number of non-US sites, would be assembled into a large scale mechanical structure, most likely at a central location in Europe. These modules would have been carefully tested, with any module specific repairs already completed at the initial module assembly site, so that the individual silicon detectors, frontend chips, and local data acquisition parts would be functional. Once assembled into a large scale structure all parts would be retested. The large scale assembly is quite challenging because of the tight alignment tolerances.

3.2.2 Pixel System

Research and development on pixel detector systems for LHC/SSC has been underway in the U.S. and Europe since the mid-1980s. Fast pixel detectors are being used in the Omega experiment at CERN [1] and will be used in the DELPHI experiment at LEP [2]. Substantial progress in R&D for LHC experiments has been made under the auspices of RD-19 [3], in addition to the work of our groups in the United States. The ATLAS pixel system design is based, in part, on these developments but represents a very significant increase in scale and complexity. Thus it is natural that some years of R&D remain, and that many, almost all, important technical choices for the pixel system remain to be made in the next few years.

The U.S. groups are now involved in most of the critical aspects of the design of the pixel system and related R&D: layout, mechanics and cooling, detectors and module design, on-detector electronics and off-detector electronics. The only important aspect in which the U.S. groups are not playing an active role is in the development of fiber optics for data transmission to and from the pixel system, which is underway by multiple groups in Europe.

The design of the ATLAS pixel system will be finalized after a 2 – 3 year R&D program that includes extensive beam tests, radiation damage studies and conceptual design and prototype fabrication. The goal of these efforts is to produce a final design with demonstrated capabilities, which addresses all of the critical technical issues, including system performance. System performance will be addressed in the Barrel Sector Prototype test in 1997, in which all elements of the barrel part of the ATLAS Inner Detector are assembled and tested together in a beam. In 1996, prototype pixel modules will be built and tested in a beam. In 1995, individual pixel arrays will undergo beam tests. The conceptual design of the pixel mechanics and cooling will occur in parallel with these beam tests. Thus by 1997, we expect all important aspects of the pixel system to be defined so that final design and subsequently fabrication and assembly can occur.

Our ongoing effort on the pixel system is intended to meet these goals. Each of our major activities is described briefly below and more details may be found in the ATLAS Technical Proposal [4] and documentation supporting that Proposal [5].

Layout

The layout of the pixel system is shown in Fig. 3.3 and the basic features have been described previously in section 3.1.1. Fig. 3.3 includes the pixel vertexing layer at a radius of about 4 cm. The major parameters of the pixel system have been summarized in Table 3.2 A number of different detailed layouts are under active investigation within ATLAS. The layout and parameters given here were developed by the U.S. groups.

Figure 3.3: A perspective view of the ATLAS pixel system

Table 3.2: Parameters of the ATLAS pixel system

Pixel size ($\phi \times z$ or R) (μm)	50×300
Number of pixels	$\sim 1.4 \cdot 10^8$
Occupancy at $\mathcal{L} = 1.0 \cdot 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$	
Pixel cell	$\sim 10^{-4}$
Pixel column	$\sim 10^{-2}$
Readout chip	~ 1
Total power (kW)	3–6

Mechanics and Cooling

We are actively working on the conceptual design of the mechanical structure and cooling system necessary to provide the layout shown in Fig. 3.3. LBL and Hytec, Inc.[1] have developed a complete conceptual model of the pixel barrel and disk mechanical structure. In the barrel region, this concept is based upon a beryllium cooling structure and a related mechanical structure. Pixel modules would be mounted on precision carbon-fiber composite carriers, which, in turn, are supported precisely at their ends by precision beryllium wheels. A model section (using brass, aluminum and silicon) has been constructed and tests are underway at LBL to measure its mechanical and thermal properties. The critical element in this design is the thermal contact between the relatively imprecise cooling tube and the carrier/silicon. Measurements will be compared with finite element thermal and mechanical models. Our present design for the disk regions includes a circumferential beryllium cooling channel that also supports the wedge-shaped silicon modules. Heat spreaders are needed to provide adequate cooling along the whole length of the silicon module, cooled near its mid-point. A thermal/mechanical prototype of this structure will also be constructed at LBL in late 1995.

Extensive finite-element thermal modeling and other thermal modeling has been done by Hytec, Inc. and this work continues. The temperature of the silicon must be maintained at 0°C or below, preferably between –10° and –5°, to minimize radiation damage effects. The preferred cooling fluid is binary ice, a suspension of small ice crystals (50–500μ diameter) in a non-aqueous medium, which is undergoing extensive evaluation at Rutherford Appleton Laboratory as the cooling medium for the silicon strip system. In addition, to the mechanical and thermal models, vibration studies have been completed for the disk structures.

The U.S. groups intend to participate fully in the conceptual design phase of the pixel mechanical and cooling system, leading to a unified design within the next two years. Once a unified design is obtained, the U.S. groups will concentrate on the detailed design of one aspect of the system (eg. the disk structures) and will collaborate with other groups (principally CPPM, Marseille) on the overall mechanical and cooling design.

[1]Hytec, Inc. is a small engineering design company located in Los Alamos, New Mexico. The owner of this company is Mr. William Miller, formerly of Los Alamos National Laboratory, who served as the lead engineer for the SDC silicon tracking subsystem.

Detectors and Modules

The readout electronics will be bump bonded to the silicon detectors that contain the pixel-array diodes. Power, data and control lines must also be brought to the readout integrated circuits and the bias voltage to the detector arrays. This can be done by using low mass cables (hybrids) connected to the silicon detectors/readout ICs and/or by using multichip module (MCM) technology to provide buses on the silicon elements themselves to route the signals. A disk module is shown in Fig. 3.4.

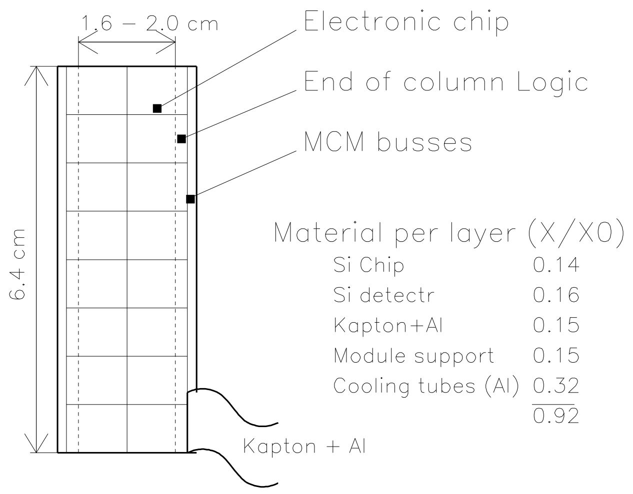

Figure 3.4: A schematic layout of a disk module

To date most of our activity has focussed on the technology needed to provide small conducting bumps on the signal pads of the pixel readout electronics and/or the pixel diode arrays. The bump spacing is 100μ and the pad sizes of interest are less than 50μ in diameter. Possible bump materials are solder, gold and indium. Indium or solder bump bonding is a relatively mature technology within the integrated circuit industry. However, the standard processes require bumps to be deposited at the wafer scale. The bumped wafers are then diced (the wafer is cut to produce the chips) and the die are mated mechanically to other ICs or, in our case, detector arrays fabricated at the LBL Microsystems Laboratory. However, to use this established process requires us to provide one or more wafers of readout electronics, an expense beyond our present means. Thus we are actively investigating two paths with industry to provide bumps on the few 2-D readout ICs (less than 25) that will be produced in the next year. One of these involves the individual deposition of small gold bumps (the process is somewhat similar to wire bonding) and the others involve the more standard evaporative or electrochemical deposition of either indium or solder/tin but on individual die. These processes are under evaluation now to bond arrays for beam tests in 1995. We are beginning to investigate the capabilities for MCM design and fabrication but work in this area, in collaboration with European groups, will only begin seriously at the end of 1995.

The pixel detectors will be exposed during their lifetimes to a particle fluence (predominantly charged hadrons) of about 10^{15} cm^{-2} and integrated doses of up to about 30 MRad.

Unlike the silicon strip system, increased noise from radiation-induced leakage current is not a major issue for the pixel system, since the capacitance of the pixel elements is so small. However, radiation damage causes the detector depletion voltage to increase and there is a practical upper limit to this voltage, about 200 V. Thinner detectors can be fully depleted longer (the depletion voltage varies as the square of the detector thickness) and thus we are forced to consider detectors as thin as 150μ for the pixel system. Thicker detectors could be used, perhaps, if successful operation of partially depleted devices could be demonstrated. Thus we have started a study of the operation of highly irradiated devices. The detector arrays and tests structures on both n- and p-type silicon have been fabricated at the LBL Microsystems Laboratory and were irradiated with 55 MeV protons in December 1994 at the LBL 88" cyclotron to a fluence that equals, approximately, 10^{15} cm^{-2} of minimum ionizing particles. Measurements of the characteristics of these devices are underway. We expect to continue to fabricate prototype detector elements in the Microsystems Laboratory and to continue to study irradiated detectors. Ultimately radiation tests must be done for both electronics and diode arrays, separately, and bonded together, to demonstrate system survivability.

We expect to fabricate a significant fraction of the pixel detector modules for the final system but the final division of module fabrication responsibilities among the ATLAS institutions is some years away. We are actively exploring the possibility of fabricating the detector arrays for these modules in the LBL Microsystems Laboratory, which could, in principle, manufacture the detector arrays we need in about a two year period.

On-Detector Electronics

The key element of the pixel system is the $\approx 2\text{m}^2$ of integrated circuits that are bump bonded to the detectors. The principal requirements for the pixel readout electronics are summarized in Table 3.3. The U.S. groups involved in pixel R&D for the SSC [6] developed some years ago the concept of a column based readout architecture for the pixel system. In this architecture, all information is transmitted along a column of pixels to logic at the end of the column and none is transmitted along the pixel rows. This minimizes the on-chip transmission of signals between pixel cells and the peripheral logic, and also reduces the inactive area (that area not covered by pixel cells). This concept has been adopted by ATLAS, although multiple schemes are under investigation to implement this architecture, and the U.S. groups are involved in the one described below. Our design has the feature of providing an analog (charge) readout which yields higher spatial precision.

In our design [see Fig. 3.5(a)] a high-speed, high-gain integrator is DC-coupled to the detector. The integrator output voltage saturates for input charges greater than about 0.3 fC and the width of the output pulse is very nearly proportional to the input charge (the design goal is 6 fC/μsec). A comparator with an adjustable threshold produces a pulse whose time-over-threshold is proportional to the input charge. This pulse is stored on a capacitor in the pixel unit cell. A few μsec long pulse (the length is adjustable) is produced to indicate that the pixel cell was hit. In addition, a narrow hit pulse (few nsec) that is ORed along the column is sent to the end-of-column (EoC) logic. The timewalk in this circuitry has been measured and simulated to be less than the 25 nsec. so that association of a hit pixel with a single beam crossing is expected, although this remains to be verified by test beam

Table 3.3: Principal requirements for the pixel detector and its readout electronics

Input threshold	~ 1000 e$^-$
Input threshold uniformity	$\pm 30\%$
Noise (after irradiation)	< 250 e$^-$
S/N - before(after) irradiation	$\sim 50(20)$
<power> per pixel (inc. logic)	< 40 μW
<readout time> per pixel	< 200 ns
Pixel deadtime (inc. readout)	$< 2\%$
Spatial resolution($R\phi$)	< 14 μm
Time between LVL1 triggers	75 ns
Mask each pixel	yes
Calibrate each pixel	yes
Max. fluence (1 MeV n equiv.)	$\sim 10^{15}$cm^{-2}
Max. ionizing dose	~ 200 kGy

Figure 3.5: A schematic view of the pixel readout circuitry

measurements. The value of a 40 MHz clock (Gray code) is latched into an event buffer in the EoC logic and the location in the event buffer is latched in the pixel unit cell using write pointers sent by the EoC logic to all cells in the column. Thus if multiple cells in a column are hit at the same time, only one location in the event buffer is used. The event buffer is deep enough so that multiple hits (different beam crossings within the L1 latency) can be stored with a negligible loss of hits.

In the current design, a hit pixel cell is automatically reset in the absence of a valid L1 accept after a fixed elapsed time. This will be modified in future iterations to latch the hit pixels until readout in coincidence with an L1 trigger with reset of others. An L1 accept, after the 2 μsec latency, initiates the readout sequence. Only pixels with a time stamp (beam crossing) matching the L1 latency may be read out, although it is also possible to read out consecutive or multiple beam crossings after the L1 accept, if desired. The matching time stamp is moved from the event buffer to an output buffer and readout of the pixels in a column begins. Pixels without data are rapidly skipped (at about 1 GHz). A hit pixel is read out in about 100 nsec. The analog information, the pixel address (row, column, chip) and the time stamp are transmitted from the readout chip.

Work on this design began in 1992, following early pixel R&D which had started in the mid 1980s. Three generations of pixel unit cell circuitry and two of the EoC logic have been fabricated, most recently in a 0.8μ, three-metal CMOS process. Three types of chips have been fabricated: 1-D arrays that contain a few examples (with different parameters) of the pixel unit cell circuitry and the interface to the end-of-column logic; chips containing the end-of-column logic; and two-dimensional arrays. All fabrication has occured through MOSIS and this will continue in 1995.

An improved EoC test chip was fabricated in late 1994 and tested in the last few months. Although it does not have the full functionality needed for a final ATLAS pixel design, it does meet the requirements for test beam work in 1995 to demonstrate the readout principle. An improved 1-D array was also fabricated in late 1994-early 1995 and tests have begun in February 1995. We expect to submit a full 2-D array to MOSIS for fabrication in March 1995. This chip, bump bonded to existing detector arrays would be used for beam tests at CERN or elsewhere in 1995.

There are a number of different designs within ATLAS to implement a column-based readout architecture. It is imperative, given the resources available to the US and to the other ATLAS groups, to achieve a unified design effort by early 1996. To this end, we have instigated a process of defining more precisely the requirements for the pixel readout, including in this process, the entire electronics chain from the pixel unit cell to the off-detector electronics. The effort to define a unified design and to appropriately apportion the electronics design responsibilities was started at an SCT meeting held at LBL in early March 1995. The goal of the U.S. groups in this area is to have a major role in the design of the pixel readout IC chip and to fabricate a substantial fraction of these chips in the U.S. to take advantage of the well developed radiation hard technologies available from multiple U.S. vendors.

3.2.3 Silicon Strip System

The first phase of the ATLAS silicon strip effort is aimed at a two year program of R&D, beam and radiation tests, commencing in 1995. The goal of these efforts will be to arrive at a final, proven system, having addressed all detector, electronics, and mechanical issues. The mechanism for demonstrating the system performance is the Barrel Sector Prototype test, expected to begin in FY96, which will have a section of all barrel tracking devices functioning together in a beam. Construction will begin following the successful performance in this test. This would involve exchange of parts so each fabrication site has all parts needed for module construction, followed by several years of module construction and test; with final full assembly at CERN.

Current Status of R&D

LBL and UCSC are presently involved in all the major technical areas involving silicon strips. The overall geometry has been described earlier. The silicon strip units are under design and a small number of options for the detectors, electronics, data readout, and module structure will be looked at in the coming year. Our particular focus to date has been in the areas of:

(*a*) Development of a bipolar frontend which can be used with either analog or digital readout. This has been a unique effort of our groups, resulting in the highest performance chip of its kind. The ATLAS groups have reached a consensus that bipolar technology is the appropriate frontend choice.

(*b*) Development of a binary digital readout chip in radiation hard CMOS technology. This has again been a unique effort, resulting in a low power, high speed, data storage chip.

(*c*) Development of modules (individual readout units made of detectors, electronics and support structure) with low mass detector-electronics interconnects. These include the investigation of Kapton and ceramic substrates.

(*d*) Development of thermal models for various module designs. This has been crucial in pinpointing possible failure modes and as guidance for the module design effort.

(*e*) Fabrication and test of detectors made from p-type silicon wafers, one of the detector options.

Our R&D to date has demonstrated the performance of the bipolar frontend and a large fraction of the digital chip in a beam test at KEK. This has involved detector units which were not irradiated. Tests with irradiated devices are now beginning (February 1995). These will culminate in a major beamtest effort at CERN in Summer 1995. ATLAS has adopted a detector readout unit which is 12 cm long and made of two bonded detector wafers; the tests at CERN will use such full length 12 cm units.

The goals for FY95 will be to quantify the performance of irradiated detectors; complete the design and testing of the radiation hard binary readout; develop an appropriate module in collaboration with the other ATLAS institutions; test detectors made from p-type wafers; and continue finite-element modeling of the cooling and support structure. We describe below in more detail the goals of the above activities.

Frontend Electronics Design

Bipolar Development We have developed a bipolar amplifier-shaper-discriminator chip which provides low noise (about 1500e including all effects) for a 15 pF detector capacitance. The chip provides 50 μm pitch readout with an adjustable power per channel which can be as low as 0.8 mW. The signal risetime, including charge collection in the detector, is 25 nsec allowing single bucket timing. These numbers have met the design goals for such a readout which we set a number of years ago. Our FY94 bipolar submission has complete calibration circuitry lacking on our earlier chips, and provides a number of chips adapted to several detector and readout options, for example AC and DC coupled detectors and analog or binary readout. Given the ATLAS consensus on using a bipolar frontend, the final chip should be very close to one of these options. It is likely that we will need one last test chip run, after final readout decisions are made, prior to production.

CMOS Development Although substantial development has been completed on the CMOS binary readout chip, which connects to the bipolar chip, it is not as far along as the bipolar development. All critical front end and storage elements have been demonstrated, but an appropriate backend needs to be completed. Functionality at 40 MHz and low power, about 0.1 mW per channel for ATLAS, have already been demonstrated. Our plan is to complete the design and performance verification using inexpensive MOSIS runs and then have one rad-hard run to provide the chips needed for a demonstration of a fully functioning radiation-hard readout for ATLAS. UCSC is chairing an ATLAS SCT committee to define the necessary backend functionality and data protocols. A proposal for a data transmission and control protocol was presented to the Inner Detector Electronics and Trigger/DAQ groups in November 1994. Recently, we completed a MOSIS submission for a Header Adder Chip (HAC) which implements part of this protocol and will be used in conjunction with our CMOS binary readout chips in the CERN beam tests this year. In addition, the interfacing of the frontend chips with the detector module must be understood and completed. This includes completing the fiber readout, developing voltage by-passing which is sufficient yet has a minimum of material, developing a power distribution system, and clarifying and minimizing the detector susceptibility to various types of failures.

Module Design and Mechanical Studies

The module plan at present [7] has two options which differ in whether the readout hybrid is mounted off the end (i.e., along the beam direction) of the detectors or off the edge. Issues of importance are the integration with the detector and cooling, cost, ease of mounting onto a mechanical structure,and material added to the detector. We expect these issues to be clarified in FY95 and will continue to contribute to these studies. This past year, we have provided initial cost estimates for the various options and have begun cooling studies. We have also begun fabrication of a Kapton version of the hybrid and bring significant experience in other substrate materials based on LBL contributions to CDF.

The work on hybrids will need to accelerate since this is the crucial interface, mechanically and electrically, of the individual detector to the external systems. Work this year has begun with construction of test boards for the CERN beamtest, leading up to the development of a fully functional hybrid. The work will involve the construction of appropriate mechanical fixtures as well as CAD layout for the boards. Decisions about appropriate materials must also be made. Our present module concept is shown in Fig. 3.6.

For the large scale mechanical structure, a design based on beryllium staves periodically stiffened by hoops has been suggested. This is shown in Fig. 3.7. We are studying the stability and deflections of such a structure. This work is being done by Hytec, Inc. In the support concept under investigation, the staves provide the cooling using binary ice, which is a promising new technique being developed at RAL in England, or more conventional liquid cooling. The control of the detector temperature is critical for running detectors after large fluences. An ideal temperature is about -5° to minimize the depletion voltage. Care with the removal of the heat generated in the detector itself is also crucial to avoid uncontrollable runaway of the detector temperature. The design of the detector modules and the design of the large scale mechanical structures must be closely coordinated efforts.

3.2.4 Off-Detector Electronics and Data Acquisition

The off-detector electronics for the silicon strips interfaces the detector modules inside the tracker with the trigger and data acquisition systems. It receives the data transmitted from the modules and delivers the data to the level 2 trigger and to the DAQ event builder. It also delivers beam clock, level 1 trigger decisions, and other control signals to the modules. The off-detector electronics manages electronics calibration and diagnostics, detector monitoring, and provides power to the on-detector electronics and bias voltages for the modules. The primary components of the off-detector electronics are readout cards which contain large memories to buffer data pending level 2 trigger decisions, embedded processors to format and preprocess the data, and the interface electronics to receive silicon tracker data over fiber optics and to transmit the data to trigger and DAQ systems over fast data links.

We are presently beginning the conceptual design of the off-detector electronics. We are also developing prototype off-detector electronics for use in upcoming beam tests of prototype silicon strip detectors and readout.

A detailed model of the data flow from the pixel system has been developed. This model is used to determine the on-detector data storage requirements, the number and bandwidth of optical fibers used to transmit data from the pixel detector to and from the off-detector electronics and the number of required off-detector readout/control cards and crates.

Data Acquisition for Beam Tests

Beam tests of irradiated detectors at KEK in the first half of FY95 and beam tests of radiation-hard readout electronics in the second half of FY95 or early FY96 require data acquisition systems to extract the data from the on-detector readout electronics. The beam tests at KEK will use a data acquisition system based on that used in previous silicon tests at KEK. When our test beam work moves to CERN, we will read out the detectors with a system based upon the data acquisition system developed for the pixel beam test program. Use of the pixel data acquisition system for the CERN silicon strip tests will begin the process of unifying the pixel and silicon readout solutions and will provide integration of our silicon readout with the overall ATLAS test beam data acquisition system. This will

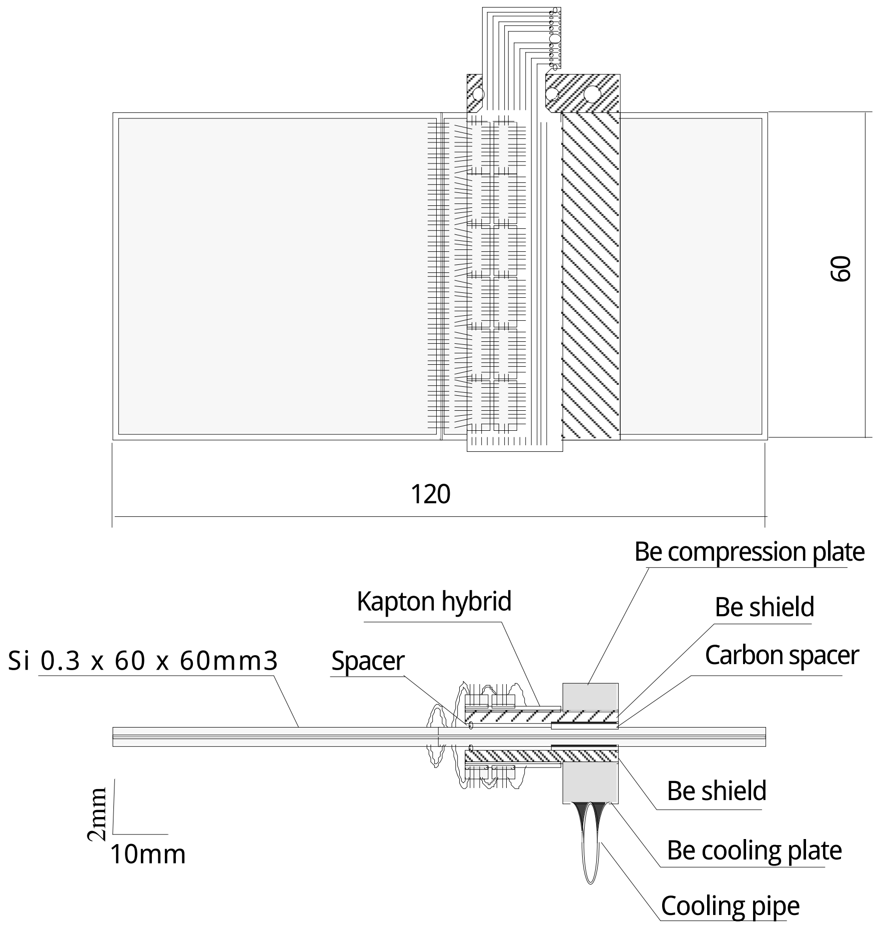

Figure 3.6: The '$R\phi$' design option for the SCT module. Note the difference in horizontal and vertical scales.

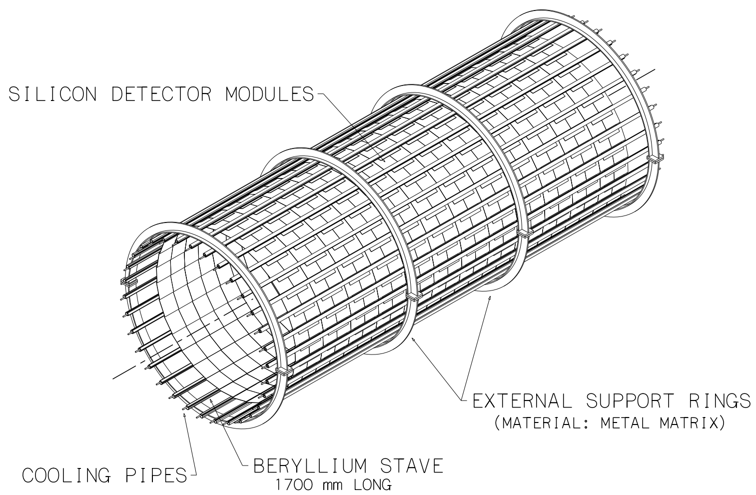

Figure 3.7: Silicon barrel at $R = 30$ cm, showing support of modules in the beryllium-stave design

provide the context for developing new off-detector logic which interfaces to the on-detector circuitry that implements the final readout protocol.

The University of Wisconsin has responsibility for design and fabrication of a readout card to hold the pixel prototypes that will undergo beam tests in 1995. This readout card is necessary to provide the digitization, data storage and trigger interface that is not part of the prototype pixel readout chip. The design of this board has been completed and fabrication has begun to support laboratory tests of the pixel readout ICs.

UC Irvine has responsibility for the design and fabrication of VME readout boards for both the pixel and silicon strip systems. These boards will contain digital signal processors, trigger control logic (different for the pixel and silicon strip systems) and other functions. The design of these boards is complete and fabrication has started to support pixel and silicon strip laboratory tests in preparation for the test beam activities later in the year. Other ATLAS groups working on different options for the silicon strip readout have expressed interest in using these boards for beam tests.

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